IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Mostafazadeh et al.	Attorney Docket No.: NSC1P275/P05654
Application No.: 10/650,215	Examiner: Not Yet Assigned
Filed: August 27 , 2003	Group: 2811
Title: DIE-LEVEL OPTO-ELECTRONIC DEVICE AND METHOD OF MAKING SAME	Confirmation No.: 7111

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on January 29, 2004 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Laura M. Dean

INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, copies of which are enclosed**, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure

** Copies of U.S. Patents and U.S. Published Applications are not enclosed.

Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NSC1P275).

Respectfully submitted,
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Form 1449 (Modified) **Information Disclosure Statement By Applicant** (Use Several Sheets if Necessary)	Atty Docket No. NSC1P275/P05654 Applicant: Mostafazadeh et al. Filing Date 08/27/2003	Application No.: 10/650,215 Group 2811

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
*	A	6,677,235	1/13/04	Yegnashankaran, et al.	438	667	12/3/2001
*	B	6,607,941	12/19/03	Prabhu, et al.	438	113	1/11/2002
*	C	6,498,381	12/24/02	Halahan, et al.	257	449	2/22/2001
*	D	6,322,903	11/27/01	Siniaguine, et al.	428	617	12/6/1999

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	E	Reche, John, "*Wafer Thinning and Thru-Silicon Vias: The Path to Wafer Level Packaging*", Tru-Si Technologies, IEEE/CPMT Meeting, Santa Clara, CA, May 10, 2000, 42 Pages.
	F	Tru-Si Technologies, "*Thru Silicon Interconnects*", 33 Pages.
	G	Advanced Semiconductor Engineering Korea, Inc., "*CMOS Image Sensor*", http://www.asekr.com/doc/ASE_korea_Image_Sensor_overview.pdf, pages 4 and 5.

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.